# riscure

driving your security forward

#### RISCURE VISION ON POST QUANTUM CRYPTOGRAPHY

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### Who is Riscure?



- Security Lab founded in the Netherlands, with branch offices in US and China
- We focus on devices that must be **secure** in a **hostile environment**
- We serve 200+ clients worldwide with security test tools, services, and training
- Our work is recognized by the world's leading security authorities

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### **1. INTRODUCTION PQC**

### **POST QUANTUM CRYPTO**

Why is this needed?

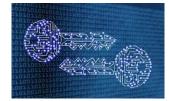
#### Quantum Computers are a field of scientific research

- using a new extremely fast method of calculation
- expected to be practical in '10' years
- Impacting cryptographic security
  - Symmetric algorithms need longer keys, i.e. 128 bit ightarrow 256 bit
  - Popular asymmetric algorithms (RSA/ECC) can be trivially broken

#### NIST

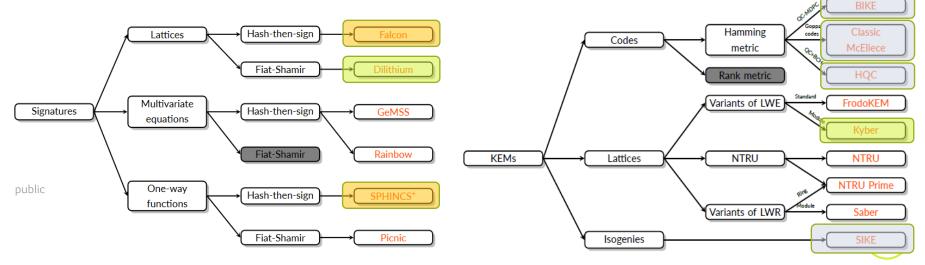
- organized (since 2016!) a contest to find the best PQC candidates
- completed the third round on in 2022
- selected algorithms for signing and key encryption, continues the search



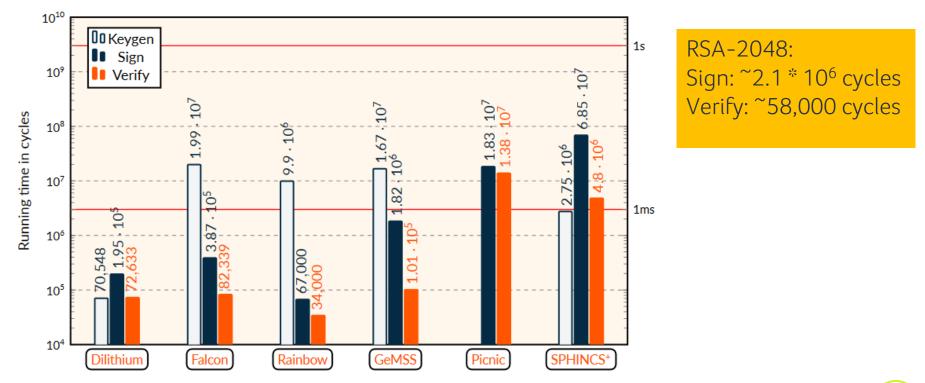


#### THE SELECTED POST QUANTUM ALGORITHMS

- Preferred algorithms are: **Dilithium** (signing) and **Kyber** (key encryption) These are fast algorithms with reasonable key/signature sizes
- 2 alternatives are given for signing: Falcon and Sphincs because of signature size, and to avoid total reliance on Lattices
- 4 additional Key encryption algorithms will be studied in Round 4



### Quantum resistant signatures - performance



PQC algorithms will likely need hardware implementation, but initial and low-cost implementations can be software based

#### **IS PQC STANDARDIZATION READY NOW?**

Stakes are growing, attacks continue

- Two recent attacks on SIKE
  - Hertzbleed, attack  $\rightarrow$  exploits "dynamic voltage & frequency scaling"
  - Glue-and-Split attack ightarrow math can break crypto in 1 hour
- SIKE is now dead 😕, but others may live 🙂
- NIST will continue the selection process
- So, how urgent is the introduction of PQC, and what are the timelines?



## **2. PQC TIMELINES**

#### WHY DO PQC IF THERE'S NO QUANTUM COMPUTER YET?

Risk	Description
Store Now, Decrypt Later	Prior to the availability of a Cryptographically Relevant Quantum Computer (CRQC), motivated bad actors may harvest data and store it, with the goal of decrypting it once quantum computing capabilities become available. This attack undermines the security of data with long-lived confidentiality needs, such as corporate IP, state secrets or individual bio-data. It is widely believed that some actors are already engaging in this type of attack.
Code-signing and Digital signatures	If algorithms become vulnerable, then service authentication can be attacked, and lead to vulnerabilities in software updates.
Rewriting history	If digital signature algorithms become vulnerable, the integrity of digitally signed data can be compromised e.g. audit records, call records, contracts, other data.
Key Management Attacks	It is possible that infrastructure is used to store symmetric keys using vulnerable wrappers. Keys used for such long-term storage can therefore become vulnerable by attacking the wrapping mechanisms.

- Encryption more urgent than signing
- Early adopters most likely governments

#### NATIONAL TIMELINES

Country	PQC Algorithms Under Consideration	Published Guidance	Timeline (summary)
China	China Specific	CACR (2020)	Start Planning
European Commission	NIST	ENISA (2022)	Start planning and mitigation
France	NIST (but not restricted to)	ANSSI (2022)	Start planning; Transition from 2025
Germany	NIST (but not restricted to)	BSI (2022)	Start planning
Japan	Monitoring NIST	CRYPTREC	Start planning; initial timeline
South Korea	KpqC	MSIT (2022)	Start competition First round (Nov.'22-Nov.'23)
United Kingdom	NIST	NCSC (2020)	Start planning;
United States	NIST	NSA (2022)	Implementation 2023-2033

#### **BUSINESS TIMELINES**

- The Global Risk Institute issued the Quantum Threat Timeline Report, stating that there is a significant (>30%) risk of a capable Quantum Computer emerging in the next decade (by 2032)
- Commercial National Security Algorithm Suite proposes a timeline



### **3. IMPLEMENTATION SECURITY**

#### **IMPLEMENTATION SECURITY**

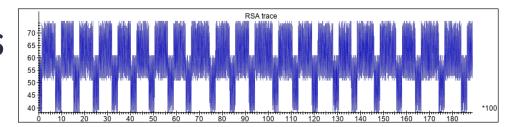
Moving to stronger algorithms only makes sense if we also address implementation security

#### Three levels of danger

- Probability
- 1. Weakness  $\rightarrow$  a theoretical situation of reduced strength (based on a threat)
  - Semiconductor work-related consumption of power
  - Semiconductor reliance on stable operating conditions
- 2. Tested vulnerability → an observable security risk (based on testing)
  - Handling of intermediate data depending on some key bits
  - Unverified output of cryptograms
- **3.** Exploit  $\rightarrow$  a practical route to compromize (based on attack)
  - CPA on S-box output
  - Horizontal Deep Learning attack on ECC

#### **HISTORY OF RSA ATTACKS**

RSA implementations have been attacked since 1997



public

- Timing
- SPA
- DPA
- CPA
- Montgomery reduction
- CRT recombination
- Templates
- Cross-correlation
- Horizontal
- Deep Learning

Exploits keep emerging, When can we be sure about implementation security?

How do we avoid PQC market disruptions due to emerging attacks?

### **4. VULNERABILITY TESTING**

#### **EFFICIENT TESTING AND REDUCING FUTURE ATTACK RISK**

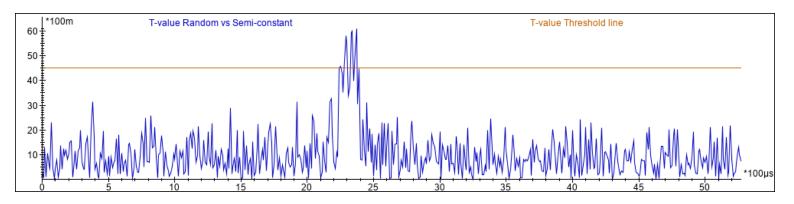
A lesson learned from certification

Focus on Vulnerabilities rather than Exploits

- Leakage assessment  $\rightarrow$  TVLA
  - testing secret leakage through Side Channel Analysis
  - only leakage measurement, no key extraction
- Robustness assessment → FIRM
  - testing chip and software robustness against Fault Injection
  - only measure corruption, no key extraction
- Vulnerability testing characteristics:
  - Fast test implementation and execution
  - May find leakage that is not (yet) exploitable (can prevent future attacks!)
  - Still need to test for all potential leakage models

#### WHAT IS TVLA?

#### Test Vector Leakage Assessment, commonly used in certification



- TVLA was proposed in 2014 by Rambus as a fast method for detecting leakage
  - saves time
  - requires less expertise
- Based on Welch's T-test, using dedicated crypto inputs, maximizing leakage of intermediate data

$$t(I) = \frac{X_{A}(I) - X_{B}(I)}{\sqrt{\frac{S_{A}^{2}(I)}{N_{A}} + \frac{S_{B}^{2}(I)}{N_{B}}}}$$

### What is FIRM?

Fault Injection Resistance Metric, under development at Riscure to increase accuracy and speed in certification

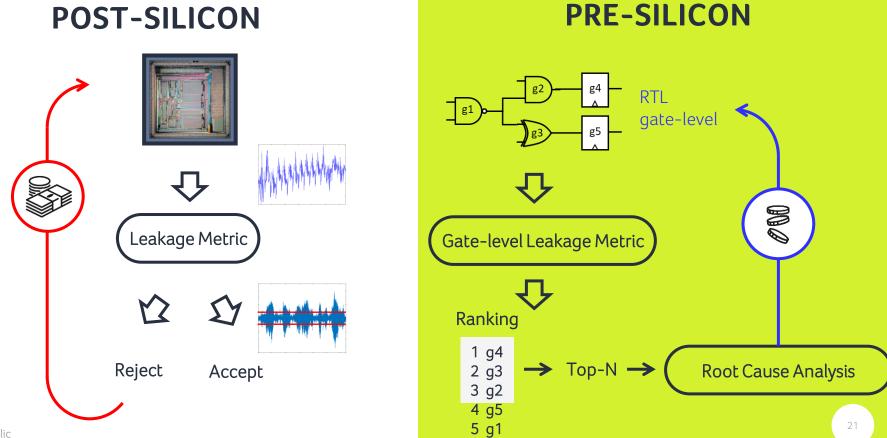
- Using dedicated target test code and test system control, testing for:
  - Wrong branch taken (if, else)
  - Instruction skipped
  - Instruction corrupted
  - Data corrupted
  - Address corrupted
  - Wild jumps due to special register (PC/RA/SP) corruption

Result	Number	Percentage	
Expected	71687	25.97%	
Crash/Mute	115036	41.68%	
CM detected	88517	32.06%	
Success	791	0.29%	

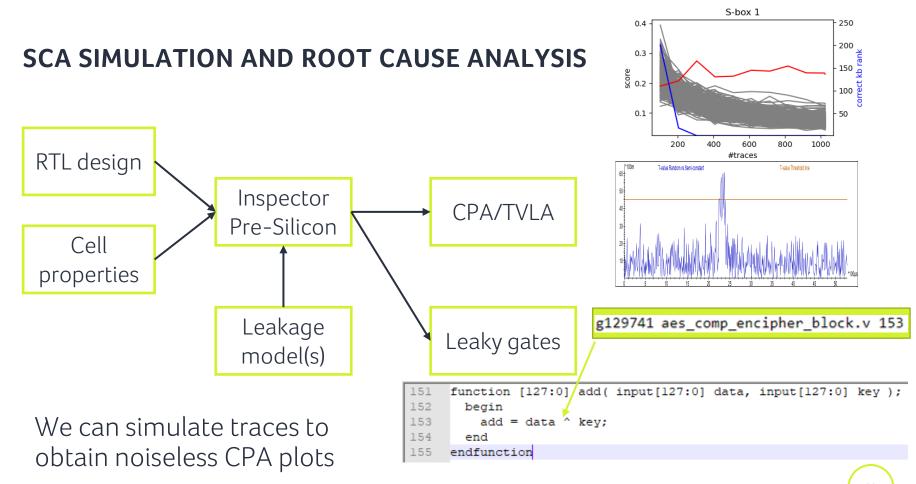
ws5-c-user 2022-01-14 16:21:30 FI-resistance-script-scheduled 1 276031 None



### **5. PRE-SILICON**



#### public



and do root cause analysis to find the leaky gates in RTL

## 6. TESTABLE INTERMEDIATE DATA IN DILITHIUM

#### WHICH INTERMEDIATES CAN WE TEST IN DILITHIUM?

$$\begin{aligned} & \frac{\operatorname{Sign}(sk, M)}{05 \ \mathbf{z} := \bot} \\ & \mathbf{06} \ \mathbf{while} \ \mathbf{z} = \bot \ \operatorname{do} \\ & \mathbf{y} \leftarrow S_{\gamma_1 - 1}^{\ell} \\ & \mathbf{08} \quad \mathbf{w}_1 := \operatorname{HighBits}(\mathbf{Ay}, 2\gamma_2) \\ & \mathbf{09} \quad c \in B_{\tau} := \operatorname{H}(M \parallel \mathbf{w}_1) \\ & \mathbf{z} := \mathbf{y} + c\mathbf{s}_1 \\ & 11 \quad \text{if } \|\mathbf{z}\|_{\infty} \ge \gamma_1 - \beta \text{ or } \|\operatorname{LowBits}(\mathbf{Ay} - c\mathbf{s}_2, 2\gamma_2)\|_{\infty} \ge \gamma_2 - \beta, \text{ then } \mathbf{z} := \bot \\ & 12 \ \text{return } \sigma = (\mathbf{z}, c) \end{aligned}$$

### **7. CONCLUSION**

#### CONCLUSION

**Riscure vision on PQC** 

- PQC implementation in HW and SW has started, but we have time to do it right!
- Vulnerability Testing is the best way to obtain security assurance because it provides efficiency and risk reduction
- Pre-silicon analysis is becoming available and can shorten time to market
- Are you building a PQC solution? Riscure can help
  - Avoid design flaws
  - Test implementation for side channel leakage and fault injection robustness
  - Get your solution certified!

#### SOURCES

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